METHOD AND APPARATUS FOR SELF-REFERENCED WAFER STAGE POSITIONAL ERROR MAPPING

ABSTRACT OF THE DISCLOSURE

A wafer stage overlay error map is created using standard overlay targets and a special numerical algorithm. A reticle including a 2-dimensional array of standard overlay targets is exposed several times onto a photoresist coated silicon wafer using a photolithographic exposure tool. After exposure, the overlay targets are measured for placement error using a conventional overlay metrology tool. The resulting overlay error data is then supplied to a software program that generates a 2-dimensional wafer stage distortion and yaw overlay error map.

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